Description

Extender Card for Testing Error–Correction–Code (ECC) Storage Area on Memory Modules

BACKGROUND OF INVENTION

[0001] This invention relates to testing of memory modules, and more particularly to testing memory modules with error-correction code (ECC) memory.

[0002] Personal computers (PC's) and other electronic systems use small printed-circuit board (PCB) daughter cards known as memory modules. Memory modules are plugged into sockets on a motherboard, reducing a need to directly mount individual memory chips on the motherboard. The memory modules are built to meet specifications set by industry standards, thus ensuring a wide potential market and low cost.

[0003] Memory modules can be tested using general-purpose electronic-component testers, but these testers tend to be quite expensive. Memory modules can also be tested in

PC-based testers. Since PC's are very inexpensive, test costs can be significantly reduced. The memory modules being tested can be inserted into memory module sockets on a PC motherboard, which executes a memory test program to test the memory modules. See as examples U.S. Patent Nos. 6178526, 6415397, 6357023, and 6,351,827.

[0004] A drawback to using a PC motherboard for testing memory modules is that the memory module sockets can become worn with use, since thousands of different memory modules may be inserted and removed for testing. The standard memory module sockets on a PC motherboard are not designed for such frequent replacement of the memory modules. Specialized test sockets such as zero-insertion-force (ZIF) sockets may replace the standard memory module sockets on PC motherboards used as testers.

[0005] Another approach is to insert an extender card into the PC motherboard's memory module socket. The memory modules are then inserted into a test socket on the extender card for testing. A higher-quality test socket can be mounted on the extender card to receive the memory modules under test.

[0006] Figures 1A-B show an extender card between a PC moth-

erboard and memory module being tested by the mother-
board. In Fig. 1A, memory module 10 contains DRAM
chips 18, 20. The number and arrangement of DRAM
chips 18, 20 vary with the memory module design and
size, and may be mounted on one or both sides of mem-
ory module 10.

[0007] Extender card 24 is a printed-circuit board (PCB) or other
substrate that has test socket 22 mounted on its upper
edge, and has metal fingers or contact pads along its bot-
tom edge. Metal wiring traces on extender card 24 con-
nect corresponding signals on the lower-edge contact
pads to metal pads in test socket 22, thus passing signals
through between PC motherboard 28 and memory module
10.

[0008] PC motherboard 28 is a larger PCB that has chips, sockets,
and other components mounted thereon, such as chip 32
and expansion sockets 36 which have expansion cards 34
plugged in. Expansion cards 34 can be Peripheral Compo-
nent Interconnect (PCI), AT-bus, or other expansion cards.
Chip 32 can be the main microprocessor, chip set, cache
memory, or other chips.

[0009] Memory module socket 26 is one of several sockets de-
signed to fit memory module 10 or other memory mod-

ules. Memory module socket 26 is mounted to the PCB substrate of PC motherboard 28, and fits the contact pads on the bottom side of extender card 24, or the contact pads on memory module 10.

[0010] Fig. 1B shows the memory module and extender card plugged into the PC motherboard. The contact pads on memory module 10 fit into test socket 22 on extender card 24. Test socket 22 can be a zero-insertion force test socket while memory module socket 26 on PC motherboard 28 is an inexpensive socket. Test socket 22 can also be a conventional memory module socket similar to memory module socket 26. The contact pads on the bottom edge of extender card 24 fit into memory module socket 26 on PC motherboard 28. Electrical contact is made by sockets 22, 26, with wiring traces on extender card 24 passing most signals through from PC motherboard 28 to memory module 10.

[0011] During testing, different memory modules 10 are repeatedly inserted into test socket 22, tested by execution of a test program on PC motherboard 28, and removed from test socket 22 and placed in a passing or a failing bin. Extender card 24 remains inserted in test socket 22 while memory module 10 is repeatedly replaced.

[0012] Figures 2A–B show testing a memory module with an error-correction code (ECC) memory using an extender card. Some memories contain redundant bits of storage for error detection and/or error correction. For example, an 8-bit-wide memory can have one extra bit, called a parity bit, for detecting an error in the 8-bit word. Memory modules can have 9 bits of data, including the parity bit and 8 data bits.

[0013] With a single parity bit, errors can only be detected, not corrected. Having additional redundant bits allows for detection and correction of simple errors. The additional bits may also allow for detection but not correction of more complex errors.

[0014] As an example, a dual-inline memory module (DIMM) may contain 64 data bits and 8 ECC bits. Memory module 10 uses a total of nine 8-bit-wide DRAM chips. Eight DRAM chips 18 store the 64 data bits while one ECC DRAM chip 20 stores the 8 ECC bits. ECC DRAM chip 20 may be located in the middle of the eight DRAM chips 18, or in some other arrangement, and some of the DRAM chips may be mounted on the back side of memory module 10, or a second bank of chips may be mounted on the back side of memory module 10.

[0015] Metal contact pads 21 on the lower edge of memory module 10 are for inserting into test socket 22 on extender card 24. Metal wiring traces on extender card 24 connect signals from test socket 22 to the corresponding signals on lower-edge contact pads 25 so that all signals are passed through unchanged, as shown in Fig. 2B.

[0016] The direct pass-through of signals from lower-edge contact pads 25 to test socket 22 and contact pads 21 allows memory module 10 to be tested just as if memory module 10 were inserted directly into memory module socket 26 on PC motherboard 28. The increased height of test socket 22 above the surface of PC motherboard 28 makes testing easier since test socket 22 is more easily reached by an operator or handler machine.

[0017] During testing of memory module 10 inserted into test socket 22, DRAM controller 38 on PC motherboard 28 receives data from a CPU or bus master and generates control signals to DRAM chips 18, 20 on memory module 10 to write the data as 64-bit words. The 64 data bits are written to DRAM chips 18 on memory module 10 by DRAM controller 38, and the 64 data bits are also sent from DRAM controller 38 to ECC generator 30 on PC motherboard 28.

[0018] ECC generator 30 generates the 8 ECC bits that are the proper correction code for the 64 data bits. The 8 ECC bits are sent to ECC DRAM chip 20 through extender card 24 to be stored with the 64 data bits at the same address in the memory module.

[0019] When the address location is read back, the 64 data bits from DRAM chips 18 are again input to ECC generator 30, and the generated ECC code is compared with the 8 ECC bits read from ECC DRAM chip 20 on memory module 10. When the generated and read-back codes mis-match, error correction is attempted, or an error is signaled. An error could occur if the DRAM chips were not refreshed quickly enough, or due to a soft error such as an alpha-particle hitting a DRAM chip.

[0020] During testing of memory module 10, a variety of specialized data patterns may be written to DRAM chips 18 and read back. These specialized data patterns have been developed to detect certain types of errors that can occur in DRAM chips, such as a single memory cell that is stuck high or low, or shorts between adjacent cells. Patterns such as walking-ones, walking-zeros, checkerboard, and inverse checkerboards are often used.

[0021] Figure 3 shows a checkerboard pattern stored in DRAM

chips on a memory module. In this simplified example, only four data DRAM chips D1, D2, D3, D4 are shown and one ECC DRAM chip "ECC" in the five columns of the Figure. Each DRAM chip is only 4 bits wide in this simplified example.

[0022] A checkerboard pattern is written to each odd address, while an inverse-checkerboard pattern is written to each even address by a test program executing on the PC motherboard. This checkerboard pattern is useful for detecting a single memory cell that is shorted to a neighboring cell, since the neighboring cells all have the opposite data state. A cell in the "1" state is surrounded by 4 cells in the "0" state.

[0023] While the checkerboard pattern is properly written to the data DRAM chips 18, the ECC DRAM chip does not necessarily contain a checkerboard pattern. This is because the ECC DRAM chip is not written by the test program. Instead, ECC DRAM chip 20 is written by ECC code generated by ECC generator 30 on PC motherboard 28. The value of the ECC code is determined by the ECC coding function, which is a function of the data bits written to data DRAM chips 18. While a variety of ECC coding functions could be used, in general the ECC code does not

look like the data pattern.

[0024] For example, the checkerboard pattern could produce the ECC value 0011 while the inverse checkerboard pattern produces an ECC value of 0001. Since the pattern of bits in ECC DRAM chip 20 is not a checkerboard, errors may be undetected in ECC DRAM chip 20.

[0025] A single memory cell in ECC DRAM chip 20 that is shorted to a neighboring cell may go undetected, since the neighboring cells do not all have the opposite data state. A cell in the "0" state might be surrounded by 1, 3, or 4 cells in the "0" state that could hide the error due to a short.

[0026] While memory modules with redundant storage are useful for error detection and correction, testing of such ECC memory modules can be problematic. A better testing procedure for use with ECC memory modules is desired. An extender card for testing ECC memory modules is also desired.

BRIEF DESCRIPTION OF DRAWINGS

[0027] Figures 1A–B show an extender card between a PC motherboard and memory module being tested by the motherboard.

[0028] Figures 2A–B show testing a memory module with an error-correction code (ECC) memory using an extender

card.

[0029] Figure 3 shows a checkerboard pattern stored in DRAM chips on a memory module.

[0030] Figure 4 shows a cross-over extender card for testing ECC memory modules.

[0031] Figure 5 shows a cross-over extender card inserted into a PC motherboard tester that is testing an ECC memory module.

[0032] Figure 6 shows a checkerboard pattern stored in DRAM chips and on the ECC DRAM chip on a memory module.

[0033] Figure 7 is a wiring diagram showing connection of signals through the cross-over extender card to the ECC memory module under test.

[0034] Figure 8 is an alternate embodiment of the cross-over extender card with a controllable mux for cross-over.

DETAILED DESCRIPTION

[0035] The present invention relates to an improvement in testing of memory modules. The following description is presented to enable one of ordinary skill in the art to make and use the invention as provided in the context of a particular application and its requirements. Various modifications to the preferred embodiment will be apparent to those with skill in the art, and the general principles de-

fined herein may be applied to other embodiments. Therefore, the present invention is not intended to be limited to the particular embodiments shown and described, but is to be accorded the widest scope consistent with the principles and novel features herein disclosed.

[0036] The inventors have realized that an extender card may be modified to improve testing of memory modules with redundant memory chips for storage of error-correction code (ECC). The modified extender card has cross-over connections to route data from the ECC generator on the PC motherboard to one of the data DRAMs, allowing data from the DRAM controller to reach the ECC DRAM. Walking-ones and zeros, checkerboard patterns, and various marching patterns can then be written into the ECC DRAM for full pattern-sensitivity testing. The ECC DRAM can be fully exercised with all the desired test patterns using the cross-over extender card.

[0037] The memory module may be tested twice – once with a standard extender card to fully test the data DRAM, and a second time with the cross-over extender card to test the ECC DRAM with the test patterns. Alternately, the cross-over connections on the cross-over extender card can be implemented with a multiplexer or switch that is con-

trolled by the test program.

[0038] Figure 4 shows a cross-over extender card for testing ECC memory modules. Cross-over extender card 44 has a PCB substrate with test socket 22 mounted to it. Wiring traces on cross-over extender card 44 connect signals from test socket 22 to the corresponding signals in lower-edge contact pads 25, except that signals from the ECC DRAM on the memory module inserted into test socket 22 are swapped with the signals from one of the data DRAMs on the memory module. For example, data signals for data DRAM chip D4 are swapped with the corresponding data signals for the ECC DRAM chip by cross-over extender card 44.

[0039] Figure 5 shows a cross-over extender card inserted into a PC motherboard tester that is testing an ECC memory module. Memory module 10 can be a dual-inline memory module (DIMM) with 64 data bits and 8 ECC bits, or can have other arrangements. In the example shown, memory module 10 uses a total of nine 8-bit-wide DRAM chips, labeled D1 to D8 and ECC. Eight DRAM chips 18 store the 64 data bits while one ECC DRAM chip 20 stores the 8 ECC bits.

[0040] Metal contact pads 21 on the lower edge of memory mod-

ule 10 are for inserting into test socket 22 on cross-over extender card 44. Metal wiring traces on cross-over extender card 44 connect signals from test socket 22 to the corresponding signals on lower-edge contact pads 25 for seven DRAM chips D1, D2, D3, D5, D6, D7, and D8. However, data signals for DRAM chip D4 are crossed over with data signals from ECC DRAM chip 20 by the wiring traces on cross-over extender card 44.

[0041] The pass-through and crossing-over of signals from lower-edge contact pads 25 to test socket 22 and contact pads 21 allows memory module 10 to be tested just as if memory module 10 were inserted directly into memory module socket 26 on PC motherboard 28, except that the ECC code is stored in data DRAM chip D4, while the data normally stored in DRAM chip D4 is instead stored in ECC DRAM chip 20.

[0042] During testing of memory module 10 inserted into test socket 22, DRAM controller 38 on PC motherboard 28 receives data from a CPU or bus master and generates control signals to DRAM chips 18, 20 on memory module 10 to write the data as 64-bit words. The 64 data bits are written to seven DRAM chips D1, D2, D3, D5, D6, D7, and D8 and to ECC DRAM chip 20 on memory module 10 by

DRAM controller 38. However, DRAM controller 38 does not write data to data DRAM chip D4.

[0043] The 64 data bits are also sent from DRAM controller 38 to ECC generator 30 on PC motherboard 28. ECC generator 30 generates the 8 ECC bits that are the proper correction code for the 64 data bits. The 8 ECC bits are sent on the ECC DRAM data lines of memory module socket 26 and lower-edge contact pads 25, and are crossed-over to the data lines for data DRAM D4 by extender card 44. The ECC code from ECC generator 30 is then sent over test socket 22 and contact pads 21 to data DRAM D4 on memory module 10.

[0044] When the address location is read back, the 64 data bits from seven DRAM chips 18 and from ECC DRAM chip 20 are again input to ECC generator 30, and the generated ECC code is compared with the 8 ECC bits read from data DRAM D4 on memory module 10. When the generated and read-back codes mis-match, error correction is attempted, or an error is signaled. An error could occur if the DRAM chips were not refreshed quickly enough, or due to a soft error such as an alpha-particle hitting a DRAM chip.

[0045] ECC DRAM chip 20 may be located in the middle of the

eight DRAM chips 18, or in some other arrangement, and some of the DRAM chips may be mounted on the back side of memory module 10, or a second bank of chips may be mounted on the back side of memory module 10. The increased height of test socket 22 above the surface of PC motherboard 28 that cross-over extender card 44 produces makes testing easier since test socket 22 is more easily reached by an operator or handler machine.

[0046] During testing of memory module 10, a variety of special-ized data patterns may be written to DRAM chips 18 and ECC DRAM chip 20 and read back. These specialized data patterns are for detecting certain types of errors that can occur in DRAM chips, such as a single memory cell that is stuck high or low, or shorts between adjacent cells. Pat-terns such as walking-ones, walking-zeros, checkerboard, and inverse checkerboards are often used.

[0047] Figure 6 shows a checkerboard pattern stored in DRAM chips and on the ECC DRAM chip on a memory module. In this simplified example, only four data DRAM chips D1, D2, D3, D4 are shown and one ECC DRAM chip "ECC" in the five columns of the Figure. Each DRAM chip is only 4 bits wide in this simplified example.

[0048] A checkerboard pattern is written to each odd address,

while an inverse-checkerboard pattern is written to each even address by a test program executing on the PC motherboard. This checkerboard pattern is useful for detecting a single memory cell that is shorted to a neighboring cell, since the neighboring cells all have the opposite data state. A cell in the "1" state is surrounded by 4 cells in the "0" state.

[0049] The checkerboard pattern is written by the DRAM controller to data DRAM chips D1, D2, and D3 but not to D4. Instead, the checkerboard pattern normally written to DRAM chip D4 is crossed-over by the cross-over extender card to be stored in the ECC DRAM chip. Thus the checkerboard pattern is written into the ECC DRAM chip. The ECC code normally written to the ECC DRAM chip is instead written to data DRAM chip D4.

[0050] DRAM chip D4 is not written by the test program. Instead, DRAM chip D4 is written by the ECC code generated by ECC generator 30 on PC motherboard 28. The value of the ECC code is determined by the ECC coding function, which is a function of the data bits written to data DRAM chips 18 and in ECC DRAM chip 20. While a variety of ECC coding functions could be used, in general the ECC code does not look like the data pattern.

[0051]   Since the ECC DRAM chip is written with the checkerboard pattern, the ECC DRAM chip can be fully tested for pattern-sensitive errors, such as single-bit errors and adjacent shorts. A single memory cell in the ECC DRAM that is shorted to a neighboring cell can be detected, since the neighboring cells all have the opposite data state. A cell in the "1" state is surrounded by 4 cells in the "0" state in ECC DRAM chip 20.

[0052]   Of course, now data DRAM chip D4 is not being fully tested, since it is not written with the checkerboard pattern, but is instead written with the ECC code. To fully test both the ECC DRAM chip and the D4 data DRAM chip, the memory module may be tested twice: once with the standard pass-through extender card 24 to test DRAM chips D1 to D8, including chip D4, and a second time with cross-over extender card 44 to test the ECC DRAM chip. The second pass using cross-over extender card 44 might not have to be as extensive since there are fewer ECC bits per address than data bits. For example, a shorter walking-ones pattern could be used for testing the ECC DRAM.

[0053]   Figure 7 is a wiring diagram showing connection of signals through the cross-over extender card to the ECC memory module under test. Power and ground lines (not

shown) from PC motherboard 28 are routed through contacts on socket 26 and wiring traces on cross-over extender card 44 to contacts on test socket 22 to power DRAM chips 18 and ECC DRAM chip 20 and other components on memory module 10, such as Phase-locked loop (PLL) buffer 62 and register 60. PLL buffer 62 receives a clock signal from PC motherboard 28 and generates CLK0 to register 60, and clock signals CLK1 to CLK8 which clock data DRAM chips 51 to 58 (D1 to D8), and clock CLK9 which clocks ECC DRAM chip 70. The many clock signals can be generated with very little skew using PLL feedback techniques when the input clock is stable.

[0054] Address and control signals from the DRAM controller on PC motherboard 28 are passed through cross-over extender card 44 and sockets 22, 26 to reach register 60 on memory module 10. Register 60 buffers and synchronizes the address and control signals before they are applied on address bus 46 to DRAM chips 51-58 and to ECC DRAM chip 70.

[0055] Each of DRAM chips 51-58 and ECC DRAM chip 70 has an 8-bit data bus, and can store data as 8-bit words, for a total of 64 data bits and 8 ECC bits per address sent over address bus 46. Data bits [0:7] from the DRAM controller

or a data buffer on PC motherboard 28 are routed to the 8 data inputs of D1 DRAM chip 51, while data bits [8:15] from the DRAM controller or a data buffer on PC motherboard 28 are routed to the 8 data inputs of D2 DRAM chip 52. Data bits [16:23] from the DRAM controller are routed to the 8 data inputs of D3 DRAM chip 53.

[0056] Similarly, data bits [32:39] from PC motherboard 28 are routed to the 8 data inputs of D5 DRAM chip 55, data bits [40:47] from PC motherboard 28 are routed to the 8 data inputs of D6 DRAM chip 56, data bits [48:55] from PC motherboard 28 are routed to the 8 data inputs of D7 DRAM chip 57, and data bits [55:63] from PC motherboard 28 are routed to the 8 data inputs of D8 DRAM chip 58. These are the direct pass-through data bits, data bits [0:23] and data bits [32:63].

[0057] Data bits [24:31] are not passed directly through. Instead, cross-over extender card 44 crosses over these bits, swapping them with the 8 ECC bits ECC[0:7]. Data bits [24:31] from PC motherboard 28 are routed over cross-over bus 48 on cross-over extender card 44 to the 8 data inputs of ECC DRAM chip 70. ECC bits ECC[0:7] from ECC generator 30 on PC motherboard 28 are routed over cross-over bus 42 on cross-over extender card 44 to the

8 data inputs of D4 data DRAM chip 54.

[0058] Thus the ECC code bits ECC[0:7] from ECC generator 30 on PC motherboard 28 are routed over cross-over bus 42 to be stored in D4 data DRAM chip 54. Data bits [24:31] from PC motherboard 28 are routed over cross-over bus 48 to be stored in ECC DRAM chip 70. The test pattern is stored in ECC DRAM chip 70, while the ECC code is stored in D4 data DRAM chip 54.

[0059] Figure 8 is an alternate embodiment of the cross-over extender card with a controllable mux for cross-over. Cross-over extender card 94 is mounted with mux switch 72. Mux switch 72 receives the 8 data bits D[24:31] and the 8 ECC bits ECC[0:7] from PC motherboard 28 through lower-edge contact pads 25. Mux switch 72 also connects to the 8 data signals for data DRAM chip D4 on memory module 10 and to the 8 data signals to the ECC DRAM chip on the memory module inserted into test socket 22.

[0060] Mux switch 72 responds to mux control signal 74, which can be generated by logic on PC motherboard 28 and applied to an otherwise unused pin on memory module socket 26 and lower-edge contact pads 25. For example, an unused pin in the interface, or an upper address bit can be used for mux control signal 74.

[0061]   When mux control signal 74 is in a first state, such as 0, Mux switch 72 passes signals directly through. Data bits D[24:31] from PC motherboard 28 are passed through mux switch 72 to the 8 data signals for data DRAM chip D4, while the 8 ECC bits ECC[0:7] are passed through to the 8 data signals to the ECC DRAM chip on the memory module. The memory module operates in a normal fashion, with the ECC code being stored in the ECC DRAM chip. The data DRAM can be written with test patterns, but the ECC DRAM chip cannot.

[0062]   When mux control signal 74 is in a second state, such as 1, Mux switch 72 crosses-over signals. Data bits D[24:31] from PC motherboard 28 are crossed over through mux switch 72 to the 8 data signals of the ECC DRAM chip. The 8 ECC bits ECC[0:7] from PC motherboard 28 are also crossed over through mux switch 72 to the 8 data signals for data DRAM chip D4. The memory module operates in a test mode, with the ECC code being stored in the D4 DRAM chip. The ECC DRAM can be written with test patterns, but the D4 DRAM chip cannot.

[0063]   A test program executing on PC motherboard 28 could first write and read test patterns to test the memory module inserted into test socket 22 of cross-over extender

card 94 by setting mux control signal 74 to 0, then switching mux control signal 74 to 1 to test the ECC DRAM chip with the test patterns.

[0064] Mux switch 72 could switch the 8 data bits, and could also switch clocking and control signals specific to the 8 data bits such as data strobes and a data mask. The timing of these control signals can be different for the data DRAM chips and the ECC DRAM chips. For example, some systems may delay writing the ECC code to the ECC DRAM to allow time for computing the ECC code.

[0065] ALTERNATE EMBODIMENTS

[0066] Several other embodiments are contemplated by the inventors. For example, a different one of the data DRAM chips could be crossed-over with the ECC DRAM chip. For example, data DRAM chip D5 could be crossed over rather than chip D4, or some other data DRAM chip could be used. The sizes of the ECC DRAM chip and the data DRAM chips do not have to be the same, and some bits in the ECC DRAM chip may be unused. Two or more data DRAM chips could be crossed-over with one ECC DRAM chip, or only some of the data lines of a DRAM chip could be crossed over to the ECC DRAM chip.

[0067] The memory module may contain additional components,

such as passive capacitors and resistors, and active components such as buffer chips, and registers for buffering control, address, or data lines.

[0068] The PC motherboard can be a standard motherboard, or can be a modified board, such as one having the socket for the extender card reverse-mounted on the solder side rather than the component side of the motherboard substrate. The PC motherboard can be one of several in a larger test system, such as in a robotic test system. A handler can automatically insert and remove the memory modules being tested, or a robotic arm or human operator can handle the memory modules under test.

[0069] More than one of the memory module slots on the PC motherboard may be loaded with an extender card, allowing two or more memory modules to be tested at the same time by the same PC motherboard. Each memory module socket or slot could have a different value of device-address lines so each slot could be accessed separately. Using two or more extender cards and slots increases testing throughput.

[0070] The cross-over extender card may be integrated with the memory module socket on the PC motherboard, or the cross-over connection may be added to the wiring or logic

on the motherboard. A standard straight–through exten-
der card or no extender card may then be used. The
cross–over extender card could have other components or
be a more complex adapter board with other functions.

[0071] Some signals or lines could be tied high or low on cross-
over extender card 44 or by the motherboard. Inverters
could be mounted on cross–over extender card 44 to in-
vert some signals or data. The data signals could include
data strobes and data mask signals, or dual–use signals
that sometimes carry data and other times carry other in-
formation, such as mask or programming information for
the DRAMs.

[0072] An unused address line could be used for the mux con-
trol, or a pre–defined data pattern or address or sequence
could be detected by logic on the cross–over extender
card and used to control the mux. A mechanical control
switch could also be used for controlling the cross–over.

[0073] Any advantages and benefits described may not apply to
all embodiments of the invention. When the word "means"
is recited in a claim element, Applicant intends for the
claim element to fall under 35 USC Sect. 112, paragraph
6. Often a label of one or more words precedes the word
"means". The word or words preceding the word "means"

is a label intended to ease referencing of claims elements and is not intended to convey a structural limitation. Such means–plus–function claims are intended to cover not only the structures described herein for performing the function and their structural equivalents, but also equivalent structures. For example, although a nail and a screw have different structures, they are equivalent structures since they both perform the function of fastening. Claims that do not use the word "means" are not intended to fall under 35 USC Sect. 112, paragraph 6. Signals are typically electronic signals, but may be optical signals such as can be carried over a fiber optic line.

[0074] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.